DIGITAL AMPLIFIER POWER STAGE

FEATURES

- 100-W RMS Power (BTL) Into 4 Ω With Less Than 10% THD+N
- 80-W RMS Power (BTL) Into 4 Ω With Less Than 0.2% THD+N
- 0.09% THD+N at 1 W Into 4 Ω
- Power Stage Efficiency Greater Than 90% Into 4-Ω Load
- Self-Protecting Design
- Industrial Temperature Rating
- 36-Pin PSOP3 Package
- 3.3-V Digital Interface
- EMI Compliant When Used With Recommended System Design

APPLICATIONS

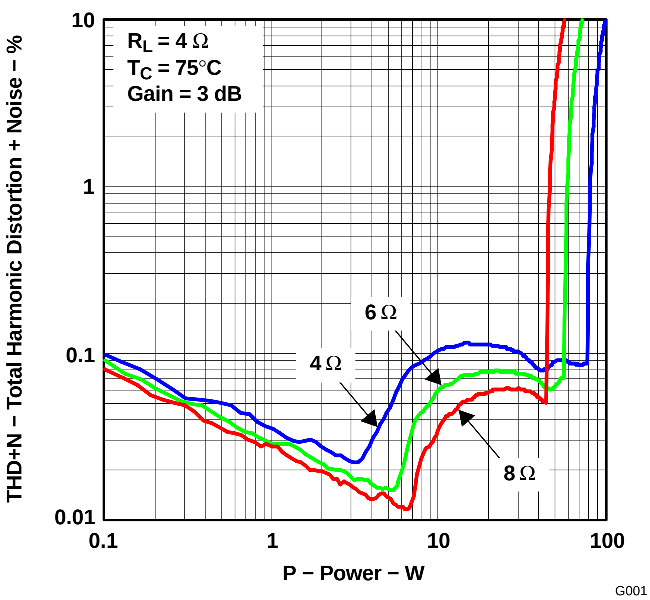
- DVD Receiver
- Home Theatre
- Mini/Micro Component Systems
- Internet Music Appliance

DESCRIPTION

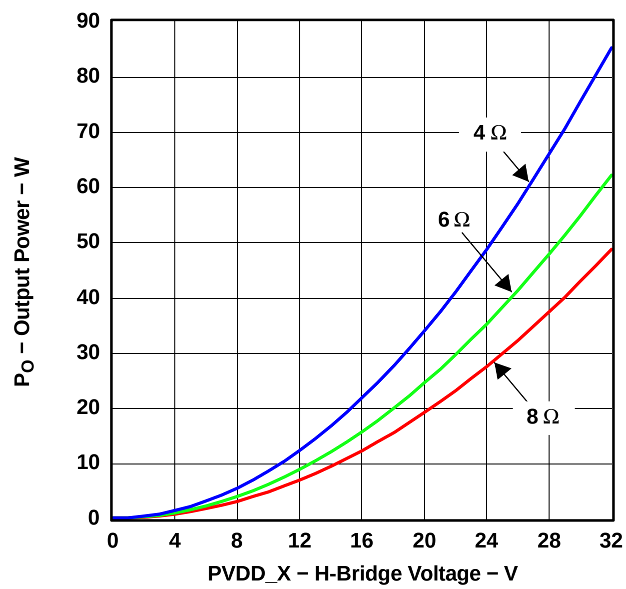
The TAS5121I is a high-performance, digital-amplifier power stage designed to drive a 4-Ω speaker up to 100 W. The TAS5121I is rated for operation at industrial temperatures. The device incorporates PurePath Digital™ technology and can be used with a TI audio pulse-width modulation (PWM) processor and a simple passive demodulation filter to deliver high-quality, high-efficiency, digital-audio amplification.

The efficiency of this digital amplifier can be greater than 90%, depending on the system design. Overcurrent protection, overtemperature protection, and undervoltage protection are built into the TAS5121I, safeguarding the device and speakers against fault conditions that could damage the system.

TOTAL HARMONIC DISTORTION + NOISE
vs
POWER



UNCLIPPED OUTPUT POWER
vs
H-BRIDGE VOLTAGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

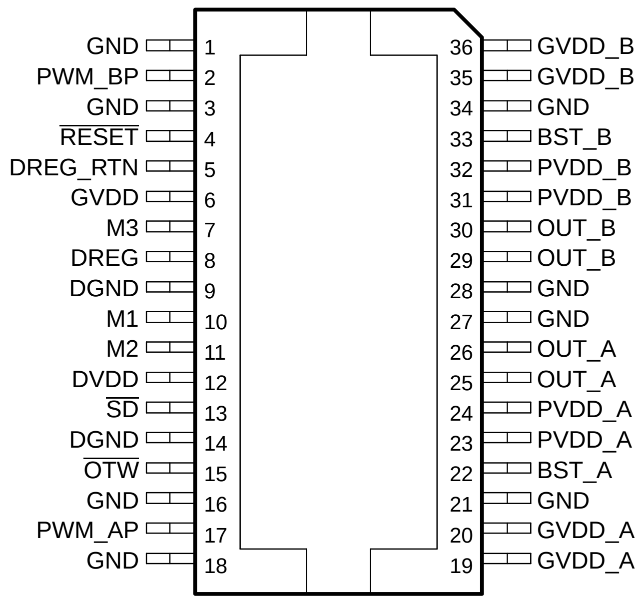
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

GENERAL INFOMATION

Terminal Assignment

The TAS5121I is offered in a thermally enhanced 36-pin PSOP3 (DKD) package. The DKD package has the thermal pad on top.

DKD PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	DVDD TO DGND	–0.3 V to 4.2 V
	GVDD_x TO GND	14.2 V
	PVDD_X TO GND (dc voltage)	33.5 V
	PVDD_X TO GND(2)	48 V
	OUT_X TO GND (dc voltage)	33.5 V
	OUT_X TO GND(2)	48 V
	BST_X TO GND (dc voltage)	46 V
	BST_X TO GND(2)	53 V
	PWM_XP, $\overline{\text{RESET}}$, M1, M2, M3, $\overline{\text{SD}}$, $\overline{\text{OTW}}$	–0.3 V to DVDD + 0.3 V
T_J	Maximum junction temperature range	–40°C to 150°C
	Storage temperature	–40°C to 125°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The duration should be less than 100 ns (see application note SLEA025).

ORDERING INFORMATION

T_A	PACKAGE	TRANSPORT MEDIA	DESCRIPTION
–40°C to 85°C	TAS5121IDKD	Tube	36-pin PSOP3
–40°C to 85°C	TAS5121IDKDR	Tape and reel	36-pin PSOP3

PACKAGE DISSIPATION RATINGS

PACKAGE	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)
36-Pin DKD PSOP3	0.85	See (1)

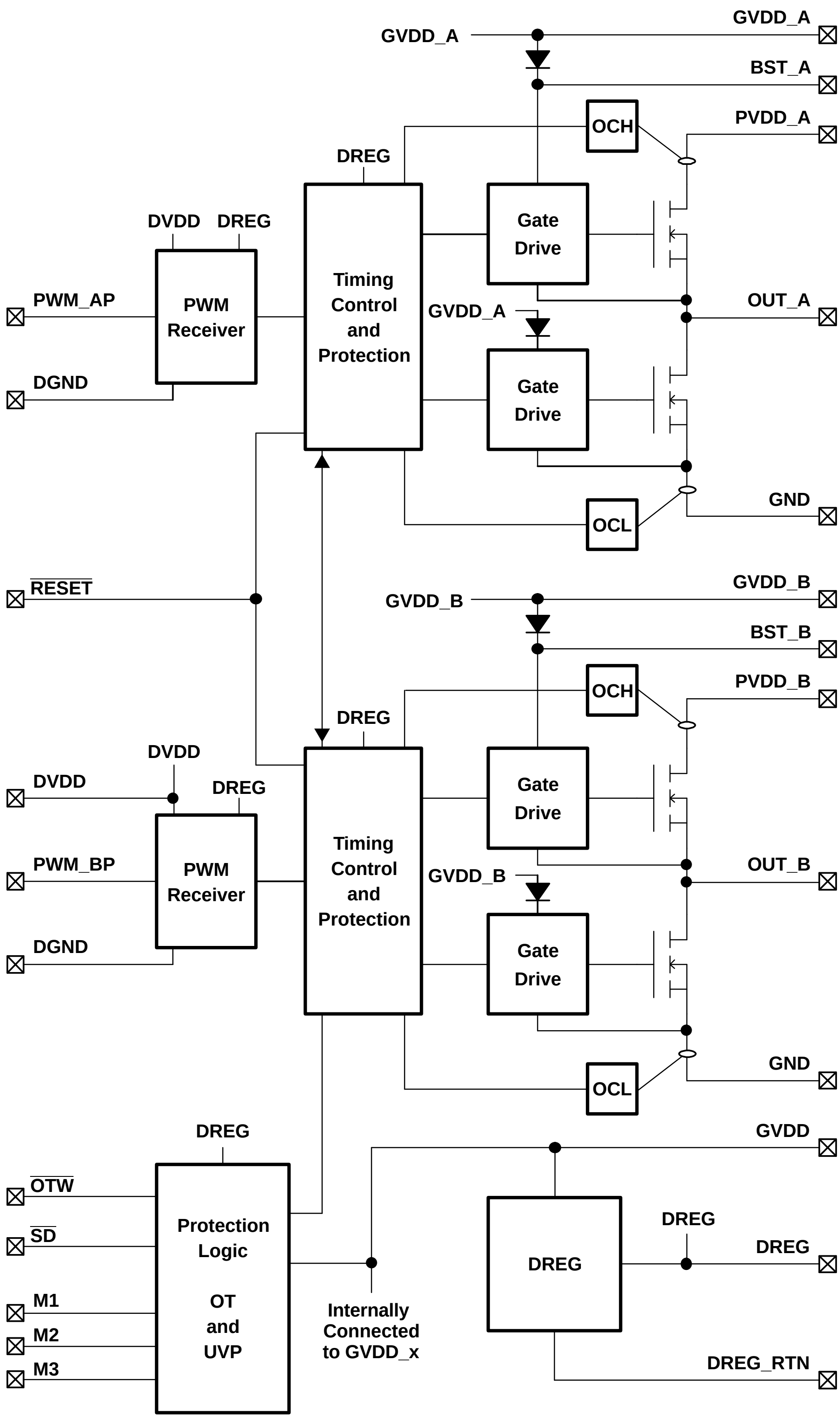
(1) The TAS5121I package is thermally enhanced for conductive cooling using an exposed metal pad area. It is impractical to use the devices with the pad exposed to ambient air as the only heat sinking of the device.
Therefore $R_{\theta JA}$, a system parameter that characterizes the thermal treatment, is provided in the *Thermal Information* section. This information should be used as a reference to calculate the heat dissipation ratings for a specific application.

Terminal Functions

TERMINAL		FUNCTION (1)	DESCRIPTION
NAME	DKD		
BST_A	22	P	High-side bootstrap (BST) supply, external resistor and capacitor to OUT_A required
BST_B	33	P	High-side bootstrap (BST) supply, external resistor and capacitor to OUT_B required
DGND	9, 14	P	I/O reference ground
DREG	8	P	Digital supply-voltage regulator-decoupling pin, 1-µF capacitor connected to DREG_RTN
DREG_RTN	5	P	Decoupling return pin
DVDD	12	P	I/O reference supply input: 100 Ω to DREG, decoupled to GND, 0.1-µF capacitor connected to GND
GND	1, 3, 16, 18, 21, 27, 28, 34	P	Power ground, connected to system GND
GVDD	6	P	Local GVDD decoupling pin
GVDD_A	19, 20	P	Gate-drive input voltage
GVDD_B	35, 36	P	Gate-drive input voltage
M1	10	I	Protection-mode selection pin, connect to GND
M2	11	I	Protection-mode selection pin, connect to DREG
M3	7	I	Output-mode selection pin; connect to GND
$\overline{\text{OTW}}$	15	O	Overtemperature warning output, open-drain with internal pullup, asserted low when temperature exceeds 115°C
OUT_A	25, 26	O	Output, half-bridge A
OUT_B	29, 30	O	Output, half-bridge B
PVDD_A	23, 24	P	Power supply input for half-bridge A
PVDD_B	31, 32	P	Power supply input for half-bridge B
PWM_AP	17	I	PWM input signal, half-bridge A
PWM_BP	2	I	PWM input signal, half-bridge B
$\overline{\text{RESET}}$	4	I	Reset signal, active-low
$\overline{\text{SD}}$	13	O	Shutdown signal for half-bridges A and B (open-drain with internal pullup)

(1) I = input, O = Output, P = Power

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
DVDD	Digital supply[(1)]	Relative to DGND	3	3.3	3.6	V
GVDD_x	Supply for internal gate drive and logic regulators	Relative to GND	10.8	12	13.2	V
PVDD_x	Half-bridge supply	Relative to GND, R_L= 4 Ω	0	30.5	32	V
T_J	Junction temperature		0		125	°C

(1) It is recommended for DVDD to be connected to DREG via a 100-Ω resistor.

ELECTRICAL CHARACTERISTICS

PVDD_X = 30.5 V, GVDD_x = 12 V, DVDD connected to DREG via a 100-Ω resistor, R_L = 4 Ω, 8X f_s= 384 kHz, TAS5026 PWM processor, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	OVER TEMPERATURE			
			T_A=25°C	T_A=25°C	T_{Case}= 75°C	UNITS	MIN/TYP/ MAX
AC PERFORMANCE, BTL Mode, 1 kHz							
P_O	Output power	R_L = 4 Ω, THD = 10%, AES17 filter			100	W	Typ
		R_L = 4 Ω, THD = unclipped, AES17 filter			80	W	Typ
		R_L = 8 Ω, THD = unclipped, AD mode			44	W	Typ
THD+N	Total harmonic distortion + noise	P_O = 1 W/channel, R_L = 4 Ω, AES17 filter			0.09	%	Typ
		P_O = 10 W/channel, R_L = 4 Ω, AES17 filter			0.15	%	Typ
		P_O = 80 W/channel, R_L = 4 Ω, AES17 filter			0.19	%	Typ
V_n	Output-integrated noise voltage	A-weighted, R_L = 4 Ω, 20 Hz to 20 kHz, AES17 filter			300	µV	Max
SNR	Signal-to-noise ratio	A-weighted, AES17 filter			95	dB	Typ
DR	Dynamic range	f = 1 kHz, –60 dB, A-weighted, AES17 filter			95	dB	Typ
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION							
DREG	Voltage regulator	I_o = 1 mA	3.3			V	Min
						V	Max
IGVDD_x	Total GVDD supply current, operating	f_S = 384 kHz, no load, 50% duty cycle	24	30		mA	Max
IDVDD	DVDD supply current, operating	f_S = 384 kHz, no load	1	5		mA	Max
OUTPUT STAGE MOSFETs							
$R_{DSon,LS}$	Forward on-resistance, low side	T_J = 25°C	120	132		mΩ	Max
$R_{DSon,HS}$	Forward on-resistance, high side	T_J = 25°C	120	132		mΩ	Max
INPUT/OUTPUT PROTECTION							
$V_{uvp,G}$	Undervoltage protection limit, GVDD		7.6	7		V	Min
				8.2		V	Max
OTW	Overtemperature warning	Static	115			°C	Typ
OTE	Overtemperature error	Static	150			°C	Typ
OC	Overcurrent protection	See [(1)].	9.5			A	Min

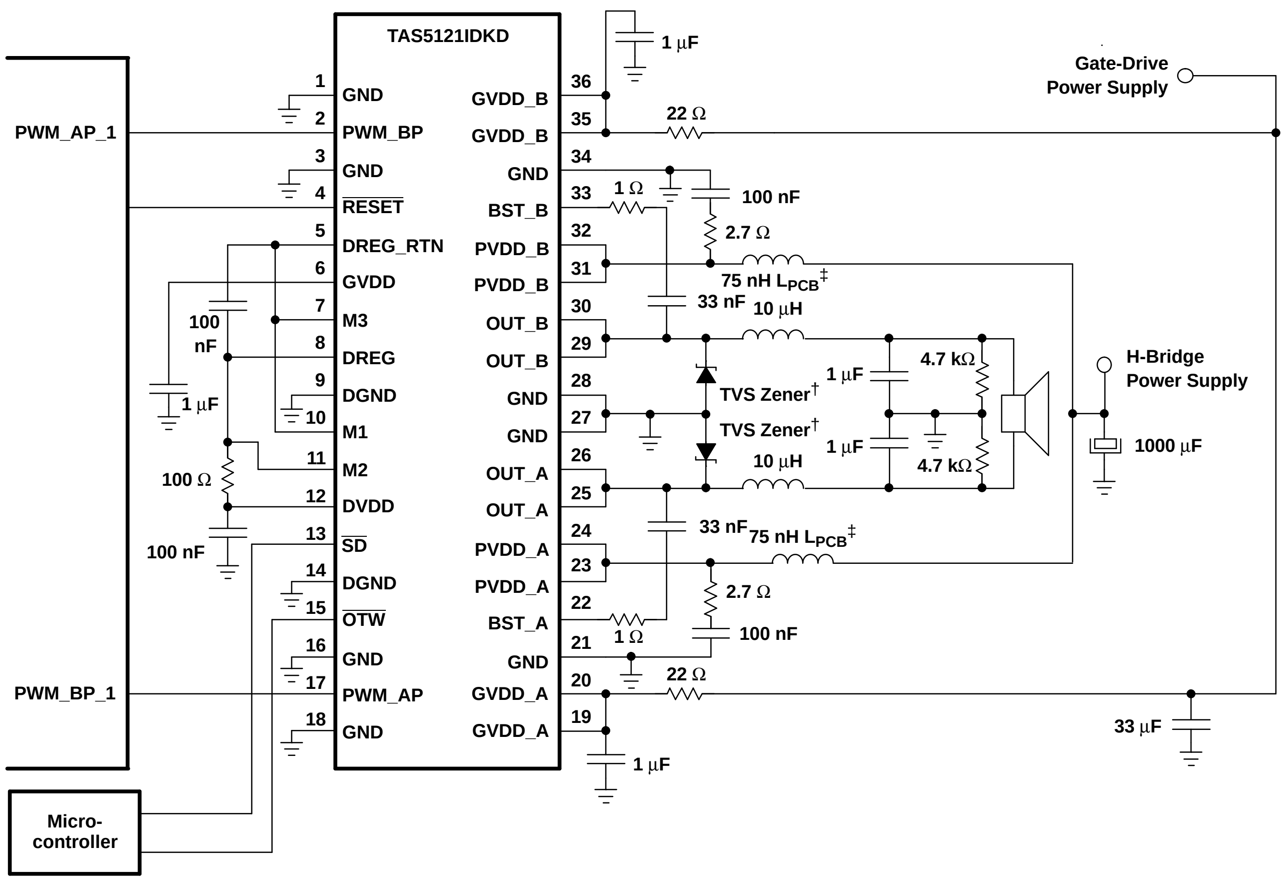
(1) To optimize device performance and prevent overcurrent (OC) protection activation, the demodulation filter must be designed with special care. See *Demodulation Filter Design* in the *Application Information* section of this data sheet and consider the recommended inductors and capacitors for optimal performance. It is also important to consider PCB design and layout for optimum performance of the TAS5121I.

ELECTRICAL CHARACTERISTICS (continued)

PVDD_X = 30.5 V, GVDD_x = 12 V, DVDD connected to DREG via a 100-Ω resistor, R_L = 4 Ω, 8X f_s= 384 kHz, TAS5026 PWM processor, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	OVER TEMPERATURE			
			T_A=25°C	T_A=25°C	T_{Case}= 75°C	UNITS	MIN/TYP/ MAX
STATIC DIGITAL INPUT SPECIFICATION, PWM, PROTECTION MODE SELECTION PINS, AND OUTPUT MODE SELECTION PINS							
V_{IH}	High-level input voltage			2		V	Min
				DVDD		V	Max
V_{IL}	Low-level input voltage			0.8		V	Max
Leakage	Input leakage current			–10		μA	Min
				10		μA	Max
OTW/SHUTDOWN (SD)							
	Internal pullup resistor from $\overline{OTW}$ and $\overline{SD}$ to DVDD		32	22		kΩ	Min
V_{OL}	Low-level output voltage	I_O = 1 mA		0.4		V	Max

TYPICAL APPLICATION CONFIGURATION USED WITH TAS5026 PWM PROCESSOR



† Voltage suppressor diodes: 1SMA33CAT3
‡ L_{PCB} : Track in the PCB (1 mm wide and 50 mm long)

S0015–01

TOTAL HARMONIC DISTORTION + NOISE
vs
POWER

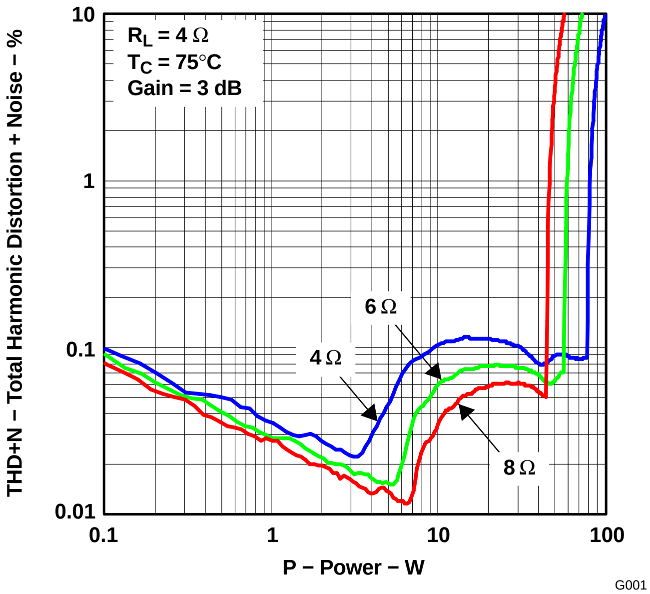


Figure 1.

UNCLIPPED OUTPUT POWER
vs
H-BRIDGE VOLTAGE

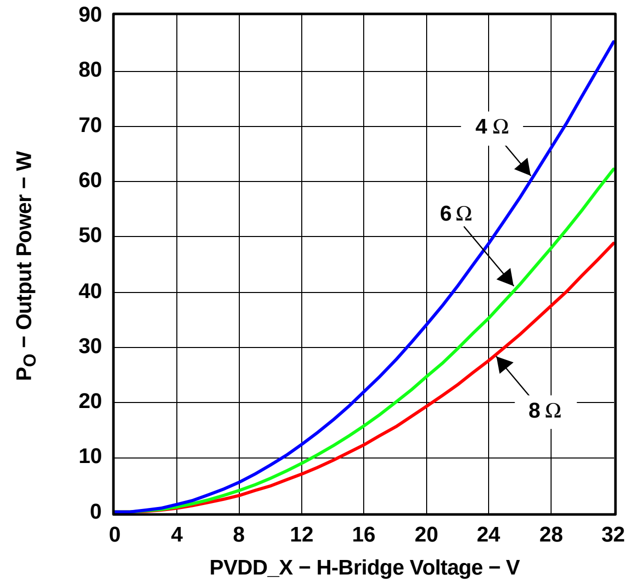


Figure 2.

POWER LOSS
vs
TOTAL OUTPUT POWER

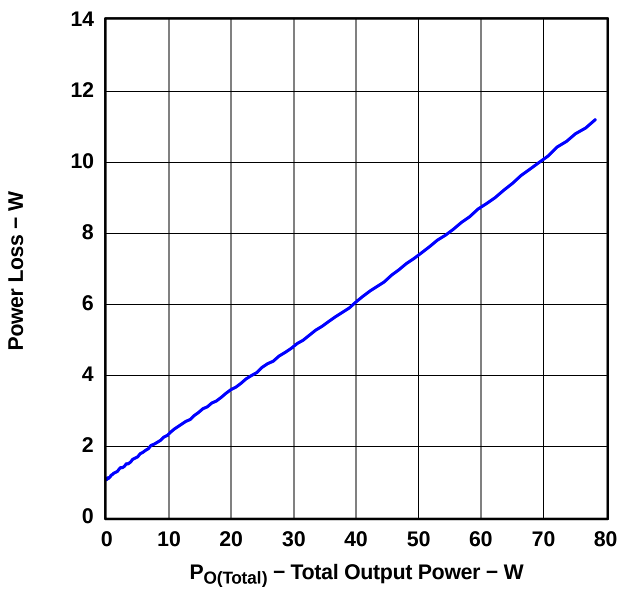


Figure 3.

UNCLIPPED OUTPUT POWER
vs
CASE TEMPERATURE

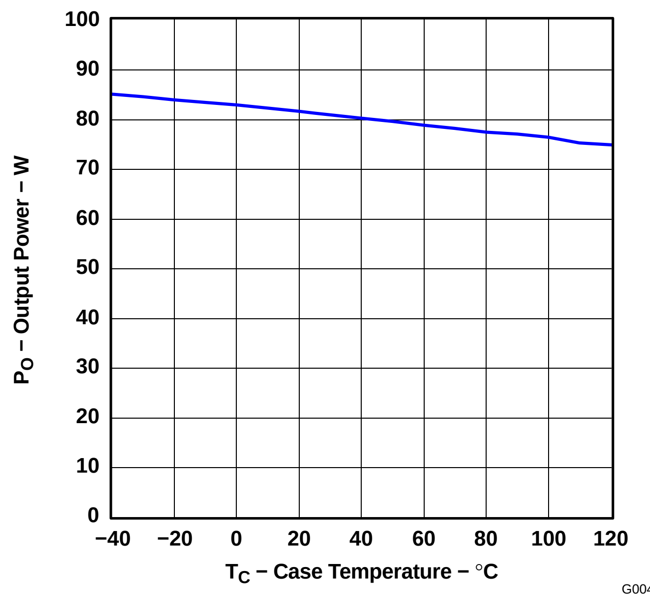


Figure 4.

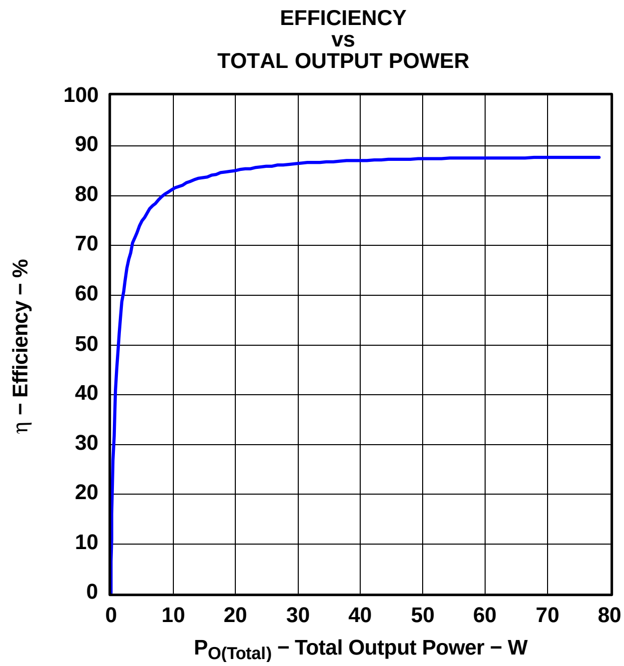


Figure 5.

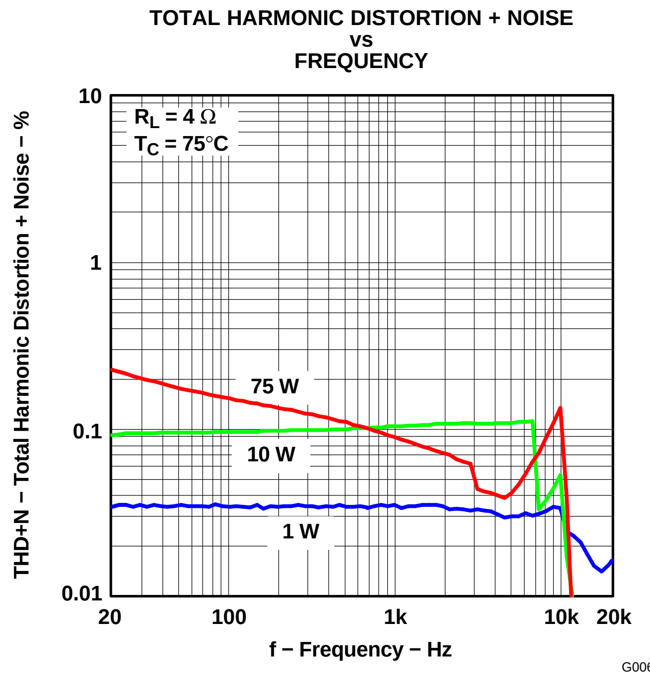


Figure 6.

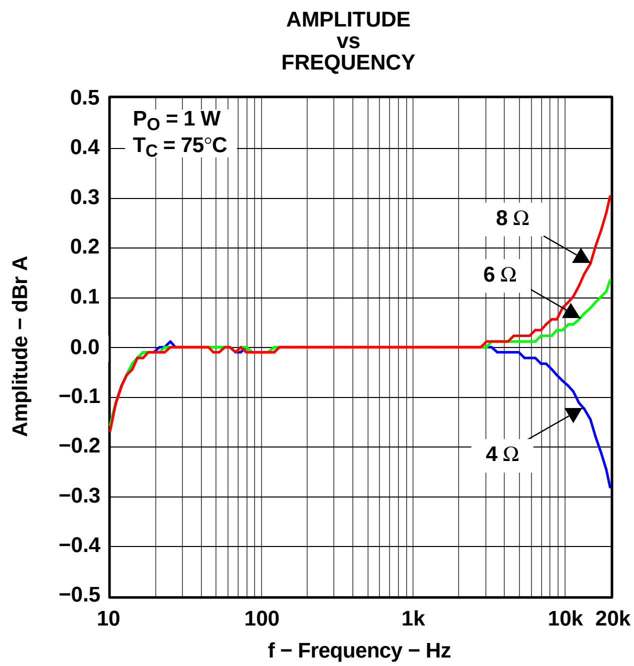


Figure 7.

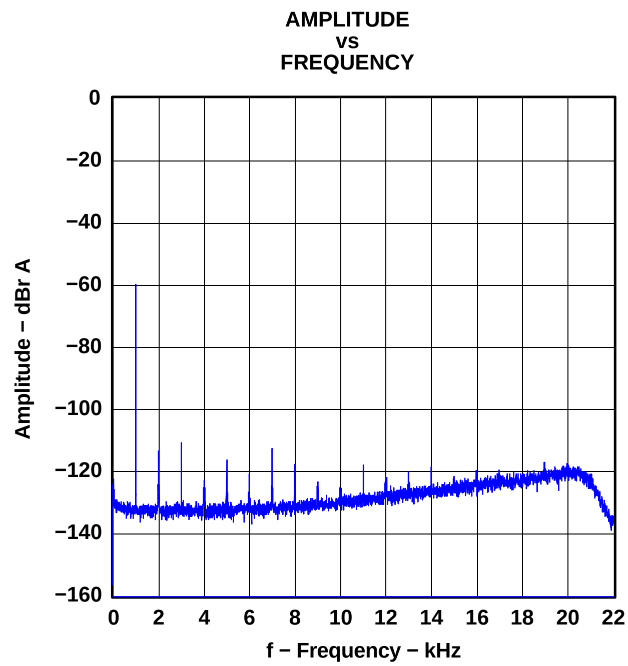


Figure 8.

THEORY OF OPERATION

POWER SUPPLIES

This power device requires only two power supply voltages: GVDD_x and PVDD_x.

GVDD_x is the gate drive supply for the device, which is usually supplied from an external 12-V power supply. GVDD_x is also connected to an internal LDR that regulates the GVDD_x voltage down to the logic power supply, 3.3 V, for the TAS5121I internal logic blocks. Each GVDD_x pin is decoupled to system ground by a 1-µF capacitor.

PVDD_x is the H-bridge power supply. Two power pins are provided for each half-bridge due to the high current density. It is important to follow the circuit and PCB layout recommendations for the design of the PVDD_x connection. For component suggestions, see the *Typical Application Configuration Used With TAS5026 PWM Processor* section in this document. Following these recommendations is important because they influence key system parameters such as EMI, idle current, and audio performance.

When GVDD_x is applied, while $\overline{\text{RESET}}$ is held low, the error latches are cleared, $\overline{\text{SHUTDOWN}}$ is set high, and the outputs are held in a high-impedance state. The bootstrap (BST) capacitor is charged by the current path through the internal BST diode and external resistors placed on the PCB from each OUT_x pin to ground.

Ideally, PVDD_x is applied after GVDD_x. When GVDD_x and PVDD_x are applied, the TAS5121I is ready for operation. PWM input signals can then be applied any time during the power-on sequence, but they must be active and stable before $\overline{\text{RESET}}$ is set high.

Recommendations for Powering Up

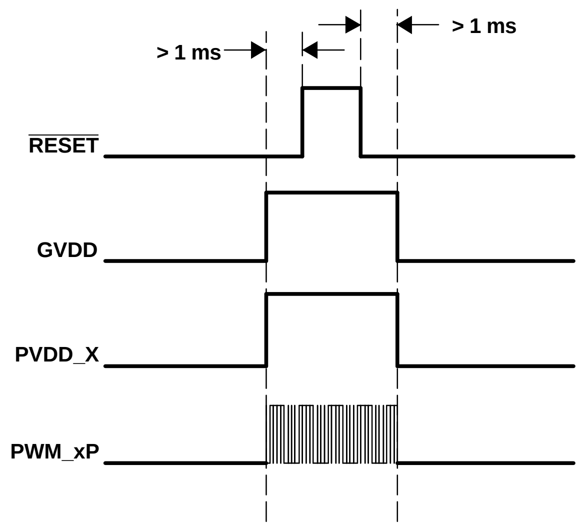


Table 1 describes the input conditions and the output states of the device.

Table 1. Input/Output States

INPUTS				OUTPUTS		CONDITION DESCRIPTION
$\overline{\text{RESET}}$	PWM_AP	PWM_BP	$\overline{\text{SHUTDOWN}}$	OUT_A	OUT_B	
X	X	X	0	Hi-Z	Hi-Z	Shutdown
0	X	X	1	Hi-Z	Hi-Z	Reset
1	0	0	1	GND	GND	
1	0	0	1	PVDD	PVDD	Normal
1	0	1	1	GND	PVDD	Normal
1	1	1	1	PVDD	PVDD	Reserved

After the previously mentioned conditions are met, the device output begins. If PWM_AP is equal to a high and PMW_BP is equal to a low, the high-side MOSFET in the A half-bridge of the output H-bridge conducts while the

THEORY OF OPERATION (continued)

low-side MOSFET in the A half-bridge is not conducting. Because the source of the high-side MOSFET is referenced to the drain of the low-side MOSFET, a bootstrapped capacitor is used to eliminate the need for additional high-voltage power supplies. Under this condition, the opposite is true for the B half-bridge of the output H-bridge. The low-side MOSFET in the B half-bridge conducts while the high-side MOSFET is not conducting; therefore, the load connected between the OUT_A and OUT_B pins has PVDD applied to it from the A side while ground is applied from the B side for the period of time PWM_AP is high and PWM_BP is low. Furthermore, when the PWM signals change to the condition where PWM_AP is low and PWM_BP is high, the opposite condition exists.

A constant high level is not permitted on the PWM inputs. This condition causes the BST capacitors to discharge and can cause device damage.

A digitally controlled dead-time circuit controls the transitions between the high-side and low-side MOSFETs to ensure that both devices in each half-bridge are not conducting simultaneously.

POWERING DOWN

For power down of the TAS5121I, an opposite approach is necessary. The $\overline{\text{RESET}}$ must be asserted LOW before the valid PWM signal is removed.

PRECAUTION

The TAS5121I must always start up in the high-impedance (Hi-Z) state. In this state, the BST capacitor is precharged by a resistor on each PWM output node to ground. See *Typical Application Configuration Used With TAS5026 PWM Processor*. This ensures that the TAS5121I is ready for receiving PWM pulses, indicating either HIGH- or LOW-side turnon after $\overline{\text{RESET}}$ is deasserted to the power stage.

With the following pulldown resistor and BST capacitor size, the BST charge time is:

- C = 33 nF, R = 4.7 kΩ
- R × C × 5 = 775.5 µs

After GVDD has been applied, it takes approximately 800 µs to fully charge the BST capacitor. During this time, $\overline{\text{RESET}}$ must be kept low. After approximately 1 ms, the power-stage BST is charged and ready. $\overline{\text{RESET}}$ can now be released if the PWM modulator is ready and is streaming valid PWM signals to the device. Valid PWM signals are switching PWM signals with a frequency between 350-400 kHz. A constant HIGH level on PWM+ forces the high-side MOSFET ON until it eventually runs out of BST capacitor energy. Putting the device in this condition should be avoided.

In practice, this means that the DVDD-to-PWM processor (modulator) should be stable, and initialization should be completed before $\overline{\text{RESET}}$ is deasserted to the TAS5121I.

CONTROL I/O

SHUTDOWN PIN: $\overline{\text{SD}}$

The $\overline{\text{SD}}$ pin functions as an output pin and is intended for protection-mode signaling to, for example, a controller or other front-end device. The pin is open-drain with an internal pullup to DVDD.

The logic output is, as shown in Table 2, a combination of the device state and $\overline{\text{RESET}}$ input.

Table 2. Error Indication

$\overline{\text{SD}}$	$\overline{\text{RESET}}$	DESCRIPTION
0	0	Reserved
0	1	Device in protection mode, i.e., UVP and/or OC and/or OT error
1 (1)	0	Device set high-impedance (Hi-Z), $\overline{\text{SD}}$ forced high
1	1	Normal operation

(1) $\overline{\text{SD}}$ is independent from $\overline{\text{RESET}}$. This is desirable to maintain compatibility with some TI PWM modulators.

OVERTEMPERATURE WARNING PIN: $\overline{\text{OTW}}$

The $\overline{\text{OTW}}$ pin gives a temperature warning signal when temperature exceeds the set limit, as shown in Table 3. The pin is of the open-drain type with an internal pullup to DVDD.

Table 3. $\overline{\text{OTW}}$ Temperature Indication

$\overline{\text{OTW}}$	DESCRIPTION
0	Junction temperature higher than 115°C
1	Junction temperature lower than 115°C

OVERALL REPORTING

The $\overline{\text{SD}}$ pin, together with the $\overline{\text{OTW}}$ pin, gives chip state information as described in Table 4.

Table 4. Error Signal Decoding

$\overline{\text{OTW}}$	$\overline{\text{SD}}$	DESCRIPTION
0	0	Overtemperature error (OTE)
0	1	Overtemperature warning (OTW)
1	0	Overcurrent (OC) or undervoltage (UVP) error
1	1	Normal operation, no errors/warnings

CHIP PROTECTION

The TAS5121I protection function is generally implemented in a closed-loop control system with, for example, a system controller. The TAS5121I contains three individual systems protecting the device against fault conditions. All of the error events result in the output stage being set in a high-impedance state (Hi-Z) for maximum protection of the device and connected equipment.

The device can be recovered by toggling $\overline{\text{RESET}}$ low and then high, after all errors are cleared. It is recommended that if the error persists, the device is held in reset until user intervention clears the error.

OVERCURRENT (OC) PROTECTION

The device has individual current protection on both high-side and low-side power-stage FETs. The OC protection works only with the demodulation filter present at the output. See *Filter Demodulation Design* in the *Application Information* section of this data sheet for design constraints.

OVERTEMPERATURE (OT) PROTECTION

A dual-temperature protection system asserts a warning signal when the device junction temperature exceeds 115°C and shuts down the device when the junction temperature exceeds 150°C. The OT protection circuit is shared by both half-bridges.

UNDERVOLTAGE PROTECTION (UVP)

Undervoltage lockout occurs when GVDD is insufficient for proper device operation. The UV protection system protects the device under fault power-up and power-down situations by shutting the device down. The UV protection circuits are shared by both half-bridges.

RESET FUNCTION

The reset has two functions:

- Reset the power stage after a latched error event.
- Hard mute—when $\overline{\text{RESET}}$ is asserted, the power stage stops switching.

In protection modes where the reset input functions as the means to re-enable operation after an error event, the error latch is cleared on the falling edge of $\overline{\text{RESET}}$, and normal operation is resumed on the rising edge of $\overline{\text{RESET}}$.

PROTECTION MODE

LATCHED SHUTDOWN ON ALL ERRORS

In latched shutdown mode, all error situations result in a permanent shutdown (output stage Hi-Z). Re-enabling can be done by toggling the $\overline{\text{RESET}}$ pin.

MODE PINS SELECTION

The protection mode is selected by connecting M1/M2 to DREG or DGND according to Table 5.

Table 5. Protection Mode Selection

M1	M2	PROTECTION MODE
0	0	Reserved
0	1	Latched shutdown on all errors
1	0	Reserved
1	1	Reserved

The output configuration mode is selected by connecting the M3 pin to DREG or DGND according to Table 6.

Table 6. Output Mode Selection

M3	OUTPUT MODE
0	Bridge-tied load output stage (BTL)
1	Reserved

APPLICATION INFORMATION

DEMODULATION FILTER DESIGN

The TAS5121I amplifier outputs are driven by high-current DMOS transistors in an H-bridge configuration. These transistors are either off or fully on.

The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. It is recommended that a second-order LC filter be used to recover the audio signal.

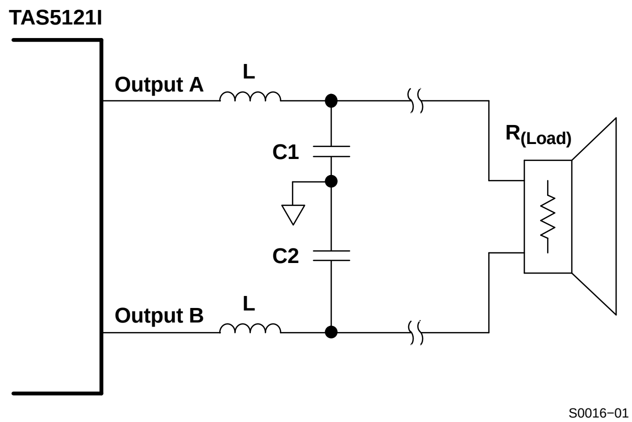


Figure 9. Demodulation Filter

The main purpose of the demodulation filter is to attenuate the high-frequency components of the output signals that are out of the audio band.

Design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to ensure proper operation of the OC protection circuit and meet the device THD+N specification, the selection of the inductors used in the output filter should be carefully considered. The rule is that the inductance should remain stable within the range of peak current seen at maximum output power and deliver approximately 5 µH of inductance at 15 A.

If this rule is observed, the TAS5121I should not have distortion issues due to the output inductors. This prevents device damage due to overcurrent conditions because of inductor saturation in the output filter.

Another parameter to be considered is the idle current loss in the inductor. This can be measured or specified as inductor dissipation (D). The target specification for dissipation is less than 0.05. If this specification is not met, idle current increases.

In general, 10-µH inductors suffice for most applications. The frequency response of the amplifier is slightly altered by the change in output load resistance; however, unless tight control of frequency response is necessary (better than 0.5 dB), it is not necessary to deviate from 10 µH.

The graphs in Figure 10 display the inductance-versus-current characteristics of two inductors that are suggested for use with the TAS5121I.

APPLICATION INFORMATION (continued)

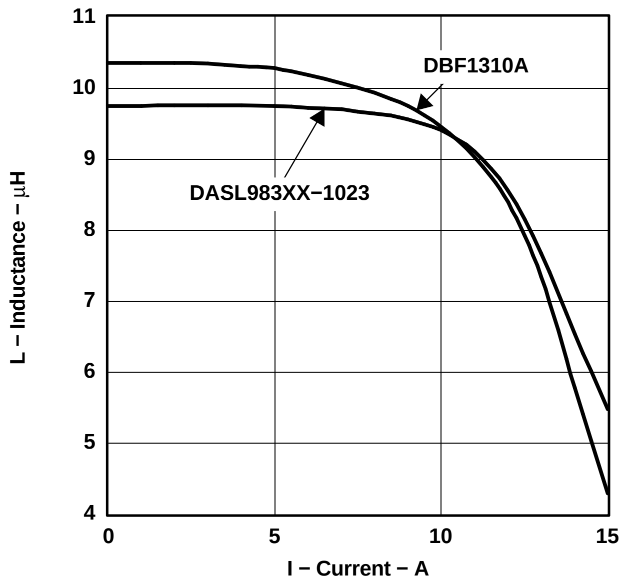


Figure 10. Inductance Saturation

The selection of the capacitors that are placed from the output of each inductor to ground is simple. To complete the output filter, use a 1-µF capacitor with a voltage rating at least twice the voltage applied to the output stage (PVDD_x).

This capacitor should be a good quality polyester dielectric.

THERMAL INFORMATION

The following information is provided as an example.

The thermally enhanced package provided with the TAS5121I is designed to be interfaced directly to a heatsink using a thermal interface compound (for example, Wakefield Engineering type 126 thermal grease.) The heatsink then absorbs heat from the ICs and transfers it to the ambient air. If the heatsink is carefully designed, this process can reach equilibrium and heat can be continually removed from the ICs without device overtemperature shutdown. Because of the efficiency of the TAS5121I, heatsinks are smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with roughly the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the metal pad)
- Heatsink compound thermal resistance
- Heatsink thermal resistance

The thermal grease thermal resistance can be calculated from the exposed pad area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W). The area thermal resistance of the example thermal grease with a 0.001-inch-thick layer is about 0.054 °C-in^2/W. The approximate exposed pad area is as follows:

36-pin PSOP3	0.116 in^2

Dividing the example thermal grease area resistance by the area of the pad gives the actual resistance through the thermal grease for the device:

APPLICATION INFORMATION (continued)

36-pin PSOP3 0.47 °C/W

The thermal resistance of thermally conductive pads is generally higher than a thin thermal grease layer. Thermal tape has an even higher thermal resistance and should not be used with this package.

Heatsink thermal resistance is generally predicted by the heatsink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus, for a single monaural IC, the system $R_{\theta JA} = R_{\theta JC}$ + thermal grease resistance + heatsink resistance.

Table 7 indicates modeled parameters for one TAS5121I IC on a heatsink. The junction temperature is set at 110°C while delivering 70 W RMS into 4-Ω loads with no clipping. It is assumed that the thermal grease is about 0.001 inch thick (this is critical).

Table 7. Example of Thermal Simulation

	36-PIN PSOP3
Ambient temperature	25°C
Power to load	70 W
Delta T inside package	5.5°C
Delta T through thermal grease	3.2°C
Required heatsink thermal resistance	11.0°C/W
Junction temperature	110°C
System $R_{\theta JA}$	12.3°C/W
$R_{\theta JA}$ * power dissipation	85°C
$R_{\theta JC}$	0.85°C/W

As an indication of the importance of keeping the thermal grease layer thin, if the thermal grease layer increases to 0.002 inches thick, the required heatsink thermal resistance increases to 5.2°C/W for the PSOP3 package.

REFERENCES

1. *Digital Audio Measurements* application report – TI (SLAA114)
2. *PowerPAD™ Thermally Enhanced Package* technical brief – TI (SLMA002)
3. *System Design Considerations for True Digital Audio Power Amplifiers* application report – TI (SLAA117)
4. *Voltage Spike Measurement Technique and Specification* application note – TI (SLEA025)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TAS5121IDKD	ACTIVE	SSOP	DKD	36	29	TBD	Call TI	Call TI
TAS5121IDKDE4	ACTIVE	SSOP	DKD	36	29	TBD	Call TI	Call TI
TAS5121IDKDR	ACTIVE	SSOP	DKD	36	500	TBD	Call TI	Call TI
TAS5121IDKDRE4	ACTIVE	SSOP	DKD	36	500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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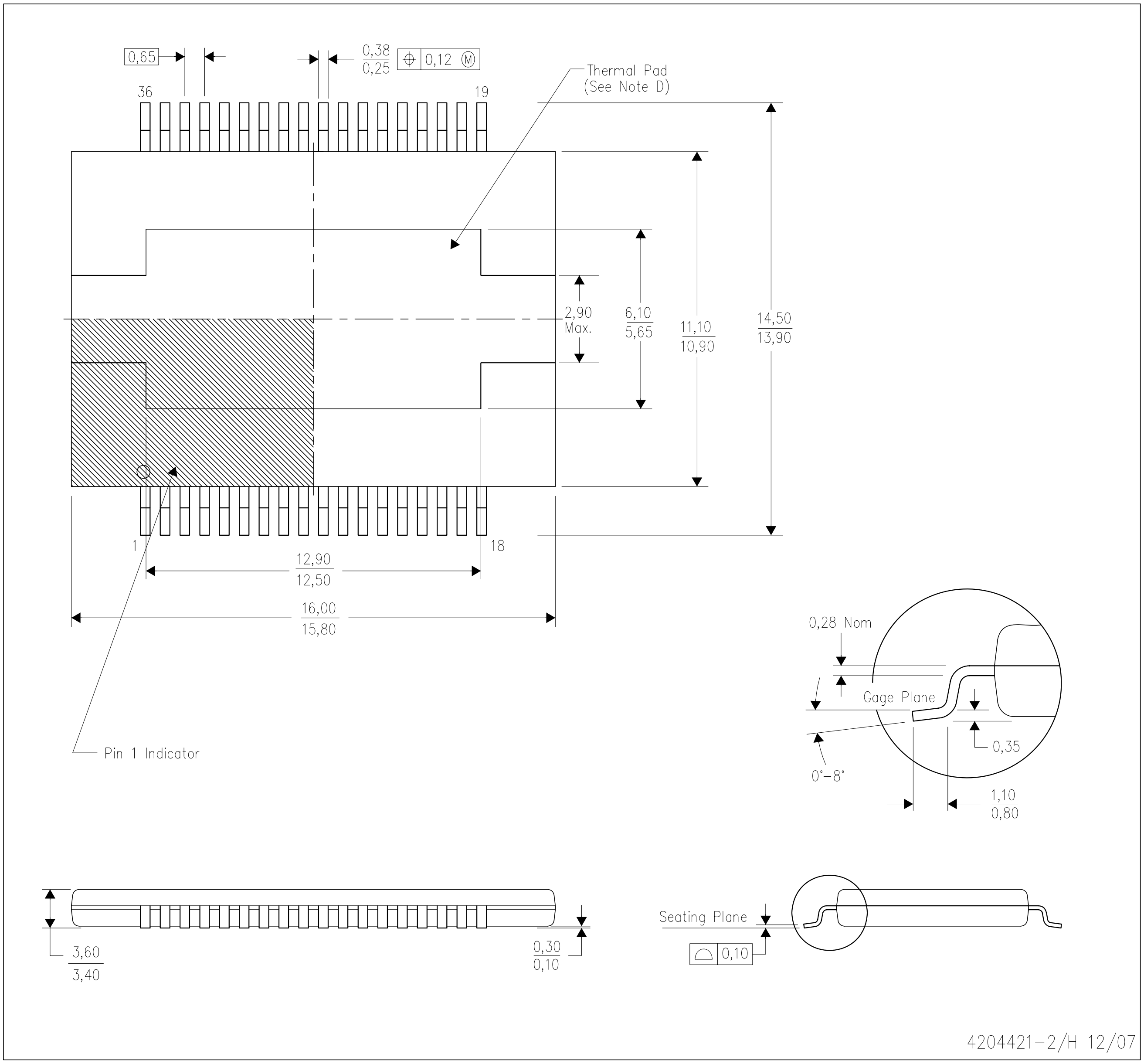
DKD (R–PDSO–G36) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.15mm.

D. The package thermal performance is optimized for conductive cooling with attachment to an external heat sink. See the product data sheet for details regarding the exposed thermal pad dimensions.